**IN THE CLAIMS**

*Please amend the claims as follows:*

1- 17. (Canceled).

18. (Currently Amended) [[The]]A semiconductor device ~~of claim 17,~~ comprising:

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit is held in the tag, selects, if the address information is not held, one of the plurality of page memory units based on preliminarily specified replacement information, releases the selected page memory unit, and transfers data from the requested address from the first memory unit into the page memory unit, and

wherein when an application under operation is changed, the replacement control unit evenly redistributes empty memories to application programs to be executed.

19. (Canceled).

20. (Original) The semiconductor device of claim 18, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.

21. (Currently Amended) [[The]]A semiconductor device ~~of claim 17,~~ comprising:

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit is held in the tag, selects, if the address information is not held, one of the plurality of page memory units based on preliminarily specified replacement information, releases the selected page memory unit, and transfers data from the requested address from the first memory unit into the page memory unit, and

wherein when an application program under operation is changed, the replacement control unit redistributes empty memories to application programs to be executed based on the priority information preliminarily defined and held in the tag.

22. (Canceled)

23. (Original) The semiconductor device of claim 21, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.

24. (Currently Amended) [[The]]A semiconductor device ~~of claim 17,~~ comprising:

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit is held in the tag, selects, if the address information is not held, one of the plurality of page memory units based on preliminarily specified replacement information, releases the selected page memory unit, and transfers data from the requested address from the first memory unit into the page memory unit, and

wherein when an application program under operation is changed, the replacement control unit redistributes empty memories to application programs to be executed in order of increasing operation cycle.

25. (Canceled)

26. (Original) The semiconductor device of claim 24, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.

27. (Currently Amended) [[The]]A semiconductor device ~~of claim 17,~~ comprising:

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit

is held in the tag, selects, if the address information is not held, one of the plurality of page memory units based on preliminarily specified replacement information, releases the selected page memory unit, and transfers data from the requested address from the first memory unit into the page memory unit, and

wherein when an application program under operation is changed, the replacement control unit redistributes empty memories to application programs to be executed in order of decreasing amount of transfer per unit time.

28. (Canceled)

29. (Original) The semiconductor device of claim 27, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.

30. (Canceled).

31. (Currently Amended) [[The]] A semiconductor device ~~of claim 30,~~ comprising

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves

as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit is held in the tag, selects, if the address information is not held, the one of the plurality of page memory units having a long access cycle, releases the selected page memory unit, and transfers data of the requested address from the first memory unit into the page memory unit, and

wherein when an application program under operation is changed, the replacement control unit evenly redistributes empty memories to application programs to be executed.

32. (Canceled)

33. (Original) The semiconductor device of claim 31, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.

34. (Currently Amended) [[The]]A semiconductor device ~~of claim 30,~~ comprising:

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit is held in the tag, selects, if the address information is not held, the one of the plurality of page memory units having a long access cycle, releases the selected page memory unit, and transfers data of the requested address from the first memory unit into the page memory unit, and

wherein when an application program under operation is changed, the replacement control unit redistributes empty memories to application programs to be executed based on the priority information preliminarily defined and held in the tag.

35. (Canceled)

36. (Original) The semiconductor device of claim 34, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.

37. (Currently Amended) [[The]]A semiconductor device ~~of claim 30,~~ comprising:

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit is held in the tag, selects, if the address information is not held, the one of the plurality of page memory units having a long access cycle, releases the selected page memory unit, and transfers data from the requested address from the first memory unit into the page memory unit, and

wherein when an application under operation is changed, the replacement control unit redistributes empty memories to application programs to be executed in order of increasing operation cycle.

38. (Canceled)

39. (Original) The semiconductor device of claim 37, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.

40. (Currently Amended) [[The]]A semiconductor device ~~of claim 30,~~ comprising:

a processor;

a first memory unit accessed by the processor and serving as a main memory;

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and is accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that each of the page memory units has a storage capacity of several kilobytes;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units, wherein

the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising a bank control unit for managing the plurality of bank memories,

the replacement control unit determines, upon receipt of an access request to any of the page memory units, whether or not information on a requested address of the page memory unit is held in the tag, selects, if the address information is not held, the one of the plurality of page memory units having a long access cycle, releases the selected page memory unit, and transfers data from the requested address from the first memory unit into the page memory unit, and

wherein when an application program under operation is changed, the replacement control unit redistributes empty memories to application programs to be executed in order of decreasing amount of transfer per unit time.

41. (Canceled)

42. (Original) The semiconductor device of claim 40, wherein the replacement control unit performs reservation and release of the page memory units in one operation cycle of the application program, does not reserve any of the empty memory during the cycle, and brings the allocated empty memory into a releasable state one cycle after.